Remarks/Arguments:

Claims 1 and 3-11 are pending in the above-identified application. Claim 1 is amended. Basis for this amendment may be found at page 7, line 20 to page 8, line 5.

Claim 1 was rejected under 35 U.S.C. § 103(a) as being obvious in view of Berenbaum et al. (U.S. Pat. No. 6,272,144 hereinafter Berenbaum), Griffin et al. (U.S. Pat. No. 5,406,403 hereinafter Griffin) and Markwalter et al. (U.S. Pat. No. 6,577,630 hereinafter Markwalter). Applicant respectfully requests reconsideration of this rejection. In particular, neither Berenbaum, Griffin, Markwalter nor their combination disclose or suggest,

> a single decoder serving the plurality of modules, the single decoder decoding the mode selection bits of the packets and providing respective mode selection signals to the plurality of modules;
>
> wherein each of the modules is operable in a reconfiguration mode in which the data portion of the packet is used by the module to change the data processing performed by the module or a processing mode in which the data portion of the packet is processed by the data processing module, responsive to the respective mode selection signal,

as required by claim 1.

In the Office Action it was admitted that "Berenbaum fails to explicitly teach [that] a module is operable in a reconfiguration mode or a processing mode responsive to a mode selection signal, a header section and a data section, a plurality of reconfigurable data processing modules, a single decoder serving a plurality of modules, a single decoder decoding bits of packets and providing signals to a plurality of modules, in which a portion of a packet is used to change data processing performed by a module." In the Office Action, Markwalter, at column 8, lines 65 through column 9, line 12, is cited as disclosing "a header section and a data section, a plurality of reconfigurable data processing modules, a single decoder serving a plurality of modules, a single decoder decoding bits of packets and providing signals to a plurality of modules, in which a portion of a packet is used to change data processing performed by a module." In particular, it is asserted that Markwalter discloses "a header section and a data section, a plurality of reconfigurable data processing modules, a single decoder serving a plurality of modules, a single decoder decoding bits of packets and providing signals to a plurality of modules in which a portion of a packet is used to change data processing performed by a module." In the Office Action, it is indicated that the RX configuration unit 72 and frame control FEC decoder 64 of Markwalter correspond to the single decoder of applicant's claim and

that the demodulator 66 and data FEC decoder 68 correspond to the plurality of modules. Applicant respectfully disagrees with this assertion.

In particular, Markwalter, at column 8, lines 37-52 recites,

> The RX configuration unit 72 receives the channel map index and the number of OFDM symbols from the frame control FEC decoder 64, retrieves from the RX channel map 78b the channel map specified by the channel map index provided by the frame control FEC decoder 64, and provides RX configuration information (derived from the channel map parameters) to the controller 76. The RX configuration information is used to configure the data FEC decoder 68 and thus includes block size and other information necessary for decoding the frame. The synchronization unit 62 provides a start-of-frame signal to the controller 76. In response to these inputs, the controller 76 provides configuration and control signals to the data FEC decoder and to the demodulator 66. For example, it conveys the modulation type associated with the received data to the demodulator 66.

Thus, the demodulator 66 and data FEC decoder 68 are externally reconfigured by the frame control and FEC decoder 64. They can not, therefore, include a "mode in which the data portion of the packet is used by the module to change the data processing performed by the module," as required by claim 1.

Furthermore, it is asserted in the Office Action that Griffin discloses a module operable in a reconfiguration mode or a processing mode. Applicant respectfully disagrees with this assertion as well. Griffin operates in a "configuration mode" not a "reconfiguration mode" as asserted in the Office Action. In this configuration mode, the apparatus disclosed by Griffin,

> includes in each data packet a data identification bit that indicates to the receiver whether the data packet is indicative of configuration information or contains transmitted data to be relayed onto the communication port associated with the receiver. If the information is configuration information the receiver stores the information in a configuration register and then compares the information in that configuration register with its own configuration to determine whether a valid connection can be obtained,

(See Griffin col. 2, lines 35-44). Thus, the information in the packet is not used by the receiver to change the data processing performed by the receiver but only to ensure that the configuration of the receiver is compatible with the configuration of the transmitter. Accordingly, Griffin can not provide the material that is missing from Berenbaum and Markwalter.

Because neither Berenbaum, Markwalter, Griffin nor their combination disclose or suggest this feature of claim 1, claim 1 is not subject to rejection under 35 U.S.C. § 103(a) in view of Berenbaum, Markwalter and Griffin.

Claims 3-7 and 11 were rejected under 35 U.S.C. § 103(a) as being obvious in view of Berenbaum, Griffin, Markwalter and further in view of the article by Laufer et al. (hereinafter Laufer). Berenbaum, Griffin and Markwalter are described above. Laufer was cited as disclosing that "a Chip ID [that] tells each chip whether to keep a header or pass it along." This, however is irrelevant to claim 3 which recites that "the frame header contains at least one mode selection bit for each of the modules." Applicant can not find this limitation in Berenbaum, Griffin, Markwalter or Laufer.

In particular, Laufer discloses a Chip ID which identifies a particular chip that the header is meant to control. This is not the same as having at least one mode selection bit for each of the modules. The use of the Chip ID requires that each module have a mechanism for recognizing when the Chip ID of a packet matches or does not match its own Chip ID. As disclosed in Fig. 4, Chip ID's are assigned as consecutive integers. Thus, the Chip ID used by Laufer can not be "at least one mode selection bit for each of the modules," as required by claim 3. The mechanism that would be used by Laufer to process the Chip ID is much more complex than a simple gating scheme that may be used by a system according to the present invention in which the single decoder merely examines the state of a respective bit in the header for each module in order to generate a respective mode selection signal for each module. Thus a system according to the present invention may be simpler than a device including a Chip ID field as disclosed by Laufer.

In addition, claim 3 depends from claim 1 and Laufer does not provide the material, described above, that is missing from Berenbaum, Griffin and Markwalter with respect to the response to the rejection of claim 1. Accordingly, claim 3 is not subject to rejection under 35 U.S.C. § 103(a) in view of Berenbaum, Griffin, Markwalter and Laufer. Claims 4 and 5 depend from claim 3 and claims 6, 7 and 11 depend from claim 1. Thus, these claims are not subject to rejection under 35 U.S.C. § 103(a) in view of Berenbaum, Griffin, Markwalter and Laufer for at least the same reasons as the claims from which they depend.

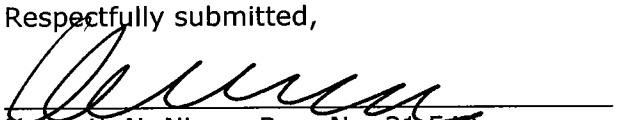
Claims 8 and 10 were rejected under 35 U.S.C. § 103(a) as being obvious in view of Berenbaum, Griffin, Markwalter and U.S. pat. no. 6,501,807 to Chieu et al. (hereinafter Chieu).

Claims 8 and 10 depend from claim 1. Berenbaum, Griffin and Markwalter are described above. Chieu discloses an RF/ID interrogator. It discloses only a single unit and, so, can not disclose or suggest the material that is missing from Berenbaum, Griffin and Markwalter, as described above. Accordingly, claims 8 and 10 are not subject to rejection under 35 U.S.C. § 103(a) as being obvious in view of Berenbaum, Griffin and Chieu for at least the same reasons as claim 1.

Claim 9 was rejected under 35 U.S.C. § 103(a) as being obvious in view of Berenbaum, Griffin and Chieu. This ground for rejection is respectfully traversed. In particular, neither Berenbaum, Griffin nor Chieu disclose or suggest that "default configuration data is supplied to at least one module of the plurality of modules from a memory outside the at least one module." In the Office Action, it is asserted that the memory 24 of Chieu meets this limitation. Applicant respectfully disagrees with this assertion. In particular, the memory 24 is disclosed as providing "program instructions utilized upon the initial start-up of the interrogator 10. It is noted that these instructions are provided to the microcontroller 22 which is in the same module 20 as the memory 24. Thus, Chieu does not disclose a memory "outside the at least one module," as required by claim 9. Consequently, the memory 24 in Chieu does not meet the limitations of claim 9 and claim 9 is not subject to rejection under 35 U.S.C. § 103(a) in view of Berenbaum, Griffin and Chieu.

In view of the foregoing amendments and remarks, Applicant requests that the Examiner reconsider and withdraw the rejection of claims 1 and 3-11.

Respectfully submitted,



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KNN/pb

Dated: January 15, 2009

The Director is hereby authorized to charge or credit Deposit Account No. **18-0350** for any additional fees, or any underpayment or credit for overpayment in connection herewith.

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